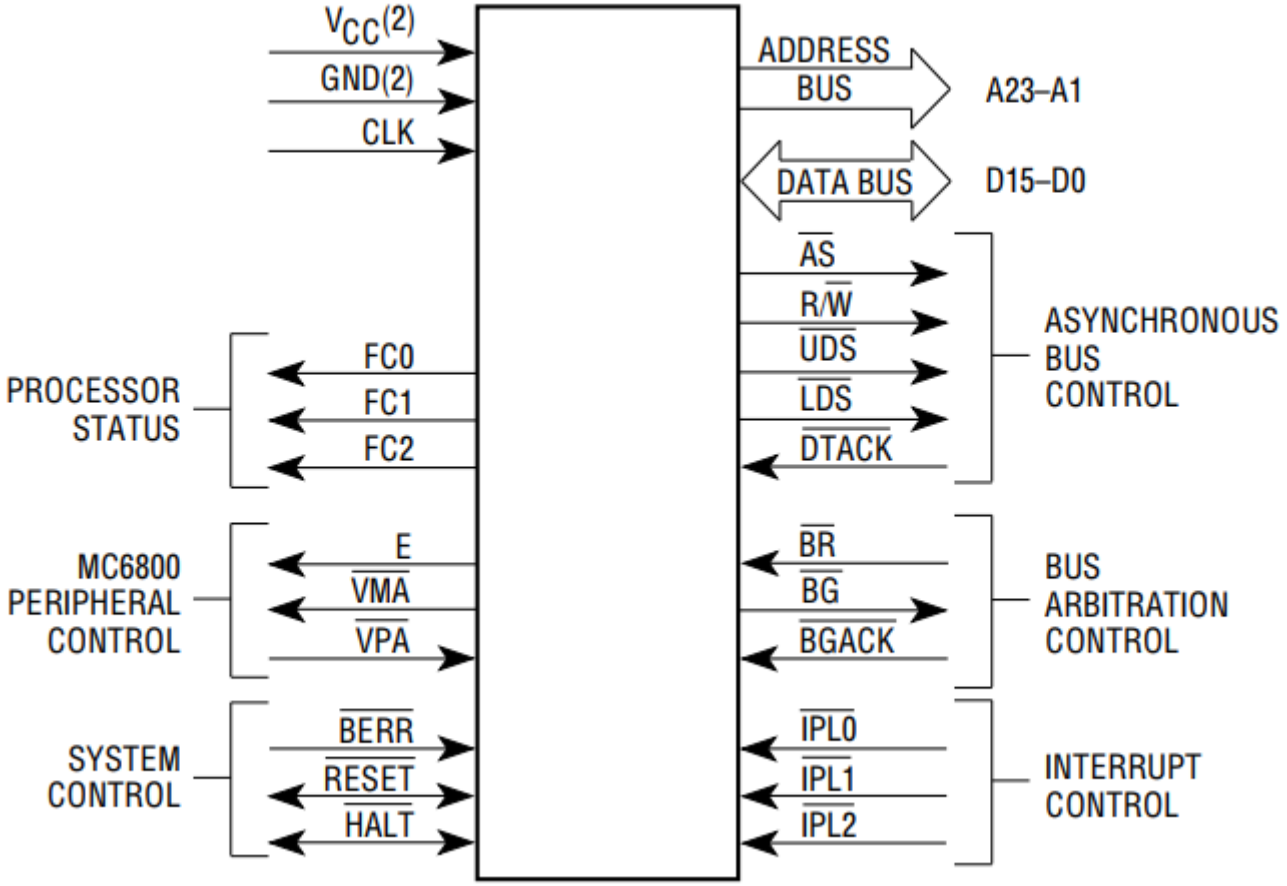
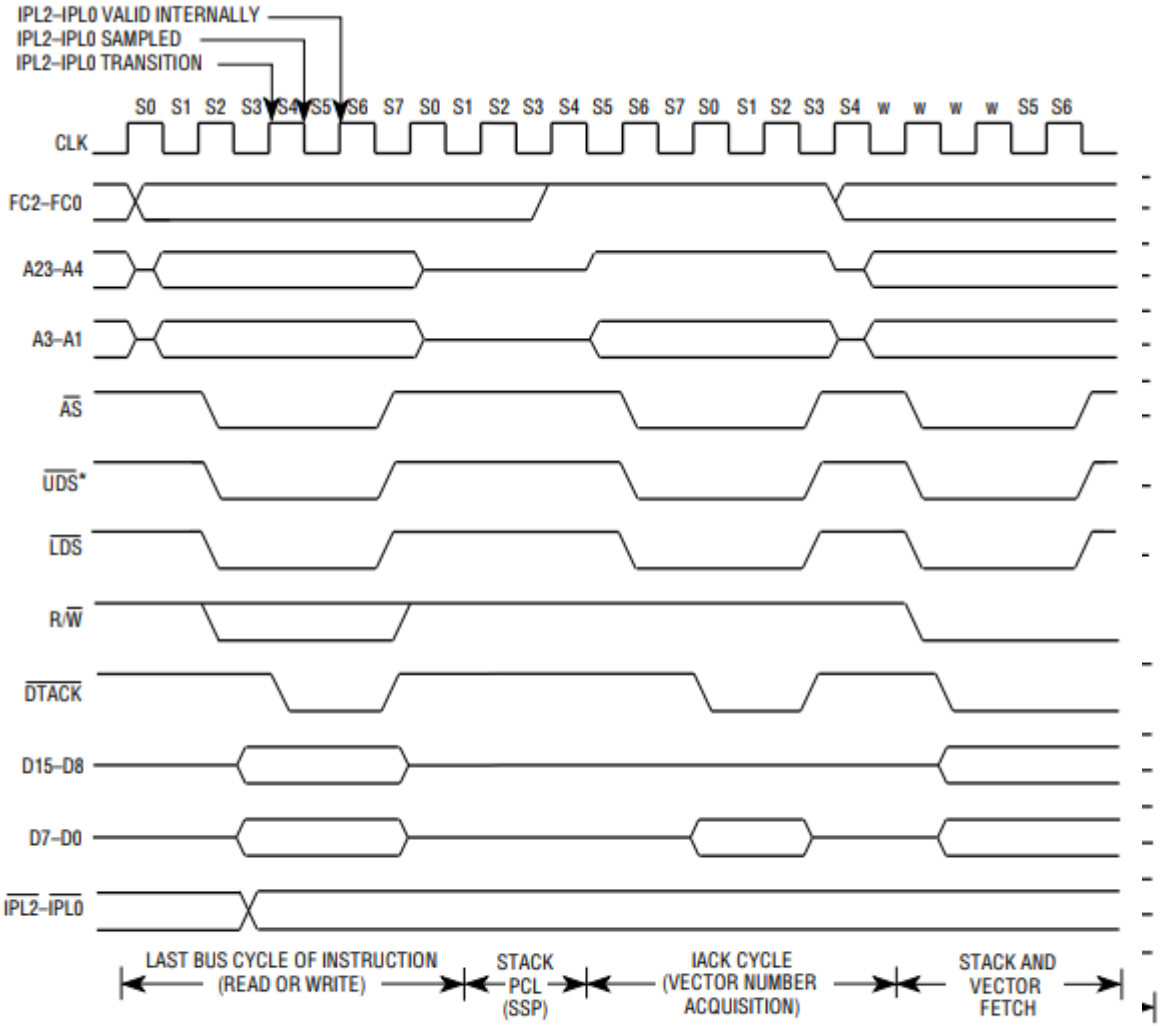

V_{CC}(2)
GND(2)
CLK
ADDRESS BUS
A23–A1
DATA BUS
D15–D0
AS
R/W
UDS
LDS
DTACK
ASYNCHRONOUS BUS CONTROL
PROCESSOR STATUS
FC0
FC1
FC2
MC6800 PERIPHERAL CONTROL
E
VMA
VPA
BR
BG
BGACK
BUS ARBITRATION CONTROL
SYSTEM CONTROL
BERR
RESET
HALT
IPL0
IPL1
IPL2
INTERRUPT CONTROL

Table 4-1. Reference Classification

Function Code Output			Reference Class
FC2	FC1	FC0	
0	0	0	(Unassigned)
0	0	1	User Data
0	1	0	User Program
0	1	1	(Unassigned)
1	0	0	(Unassigned)
1	0	1	Supervisor Data
1	1	0	Supervisor Program
1	1	1	Interrupt Acknowledge

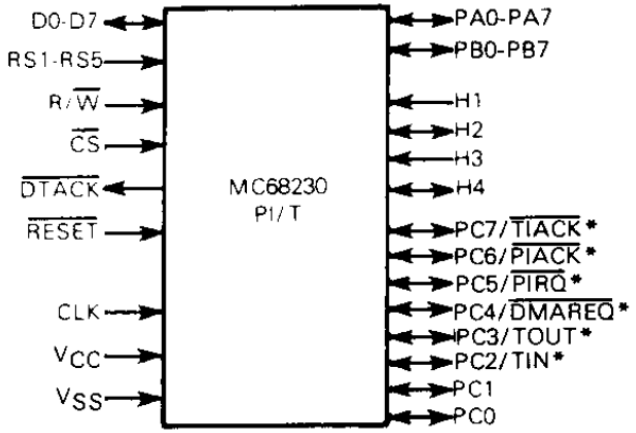
Table 4-2. Exception Vector Assignment

Vector Number(s)	Dec	Address Hex	Space	Assignment
0	0	000	SP	Reset: Initial SSP[2]
1	4	004	SP	Reset: Initial PC[2]
2	8	008	SD	Bus Error
3	12	00C	SD	Address Error
4	16	010	SD	Illegal Instruction
5	20	014	SD	Zero Divide
6	24	018	SD	CHK Instruction
7	28	01C	SD	TRAPV Instruction
8	32	020	SD	Privilege Violation
9	36	024	SD	Trace
10	40	028	SD	Line 1010 Emulator
11	44	02C	SD	Line 1111 Emulator
12[1]	48	030	SD	(Unassigned, Reserved)
13[1]	52	034	SD	(Unassigned, Reserved)
14	56	038	SD	Format Error[5]
15	60	03C	SD	Uninitialized Interrupt Vector
16-23[1]	64	040	SD	(Unassigned, Reserved)
	95	05F		—
24	96	060	SD	Spurious Interrupt[3]
25	100	064	SD	Level 1 Interrupt Autovector
26	104	068	SD	Level 2 Interrupt Autovector
27	108	06C	SD	Level 3 Interrupt Autovector
28	112	070	SD	Level 4 Interrupt Autovector
29	116	074	SD	Level 5 Interrupt Autovector
30	120	078	SD	Level 6 Interrupt Autovector
31	124	07C	SD	Level 7 Interrupt Autovector
32-47	128	080	SD	TRAP Instruction Vectors[4]
	191	0BF		
48-63[1]	192	0C0	SD	(Unassigned, Reserved)
	255	0FF		—
64-255	256	100	SD	User Interrupt Vectors
	1023	3FF		—



*Although a vector number is one byte, both data strobes are asserted due to the microcode used for exception processing. The processor does not recognize anything on data lines D8 through D15 at this time.

Figure 5-11. Interrupt Acknowledge Cycle Timing Diagram



*Individually Programmable Dual-Function Pin

Table 1-3. Register Model (Sheet 1 of 2)

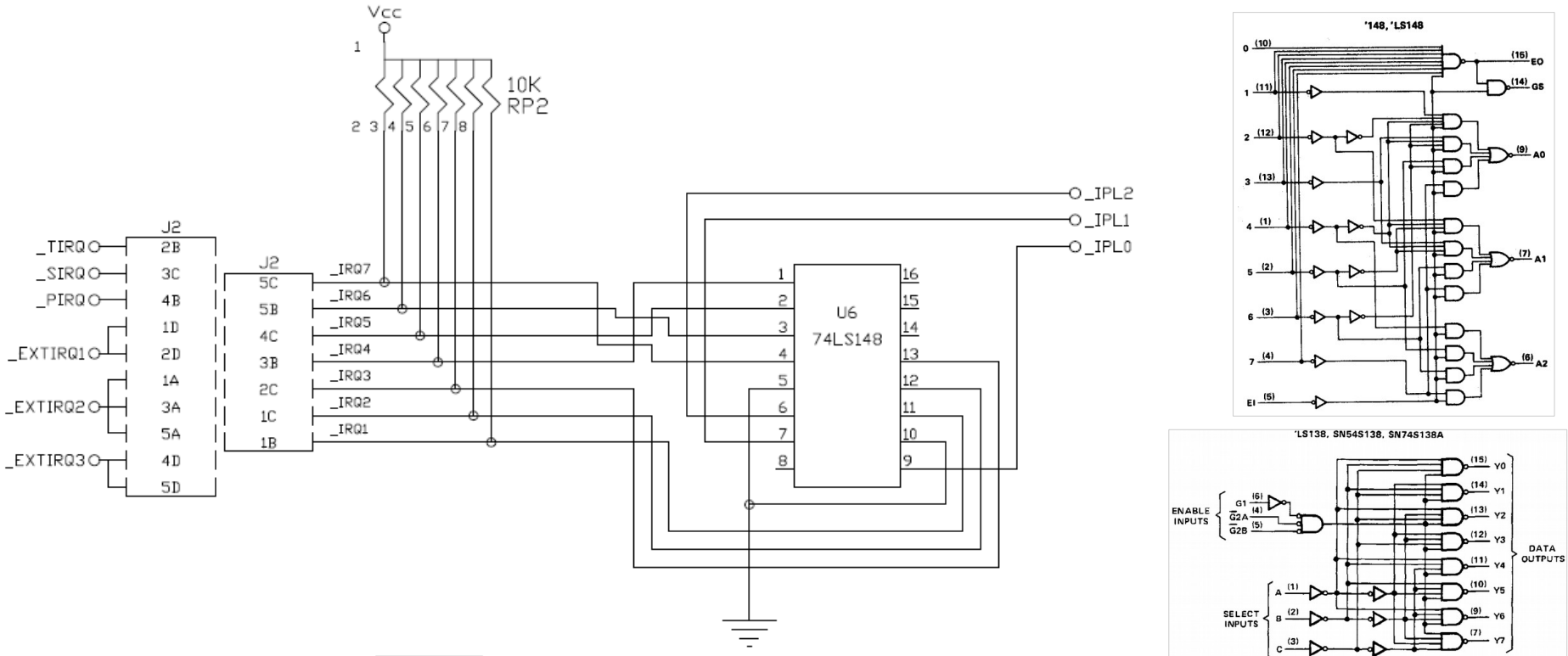
Register Select Bits 5 4 3 2 1	7	6	5	4	3	2	1	0	Register Value After RESET (Hex Value)	
0 0 0 0 0	Port Mode Control		H34 Enable	H12 Enable	H4 Sense	H3 Sense	H2 Sense	H1 Sense	0 0	Port General Contol Register
0 0 0 0 1	*	SVCRQ Select		IPF Select		Port Interrupt Priority Control			0 0	Port Service Request Register
0 0 0 1 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	0 0	Port A Data Direction Register
0 0 0 1 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	0 0	Port B Data Direction Register
0 0 1 0 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	0 0	Port C Data Direction Register
0 0 1 0 1	Interrupt Vector Number						*	*	0 F	Port Interrupt Vector Register
0 0 1 1 0	Port A Submode		H2 Control			H2 Int Enable	H1 SVCRQ Enable	H1 Stat Ctrl	0 0	Port A Control Register
0 0 1 1 1	Port B Submode		H4 Control			H4 Int Enable	H3 SVCRQ Enable	H3 Stat Ctrl	0 0	Port B Control Register
0 1 0 0 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	**	Port A Data Register
0 1 0 0 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	**	Port B Data Register
0 1 0 1 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	***	Port A Alternate Register
0 1 0 1 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	***	Port B Alternate Register
0 1 1 0 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	****	Port C Data Register
0 1 1 0 1	H4 Level	H3 Level	H2 Level	H1 Level	H4S	H3S	H2S	H1S	****	Port Status Register
0 1 1 1 0	*	*	*	*	*	*	*	*	0 0	(Null)
0 1 1 1 1	*	*	*	*	*	*	*	*	0 0	(Null)

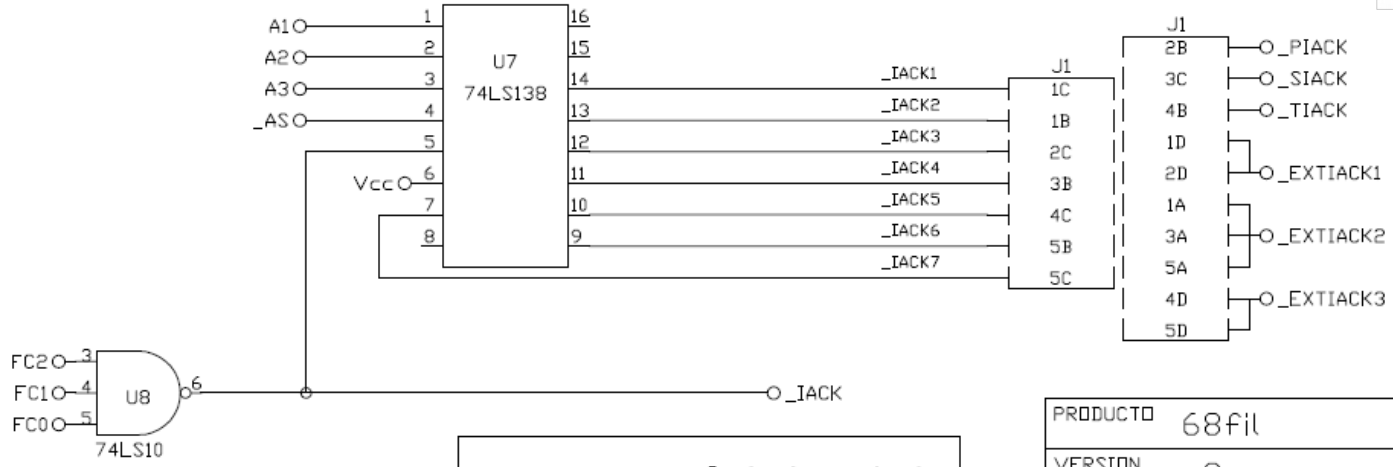
*Unused, read as zero
**Value before RESET
***Current value on pins
****Undetermined value

Table 1-3. Register Model (Sheet 2 of 2)

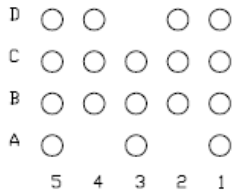
Register Select Bits 5 4 3 2 1	7	6	5	4	3	2	1	0	Register Value After RESET (Hex Value)	
1 0 0 0 0	TOUT/TIACK Control			Z D Ctrl	*	Clock Control		Timer Enable	0 0	Timer Control Register
1 0 0 0 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	0F	Timer Interrupt Vector Register
1 0 0 1 0	*	*	*	*	*	*	*	*	0 0	(Null)
1 0 0 1 1	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	**	Counter Preload Register (High)
1 0 1 0 0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	**	Counter Preload Register (Mid)
1 0 1 0 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	**	Counter Preload Register (Low)
1 0 1 1 0	*	*	*	*	*	*	*	*	0 0	(Null)
1 0 1 1 1	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	**	Count Register (High)
1 1 0 0 0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	**	Count Register (Mid)
1 1 0 0 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	**	Count Register (Low)
1 1 0 1 0	*	*	*	*	*	*	*	ZDS	0 0	Timer Status Register
1 1 0 1 1	*	*	*	*	*	*	*	*	0 0	(Null)
1 1 1 0 0	*	*	*	*	*	*	*	*	0 0	(Null)
1 1 1 0 1	*	*	*	*	*	*	*	*	0 0	(Null)
1 1 1 1 0	*	*	*	*	*	*	*	*	0 0	(Null)
1 1 1 1 1	*	*	*	*	*	*	*	*	0 0	(Null)

*Unused, read as zero
**Value before RESET



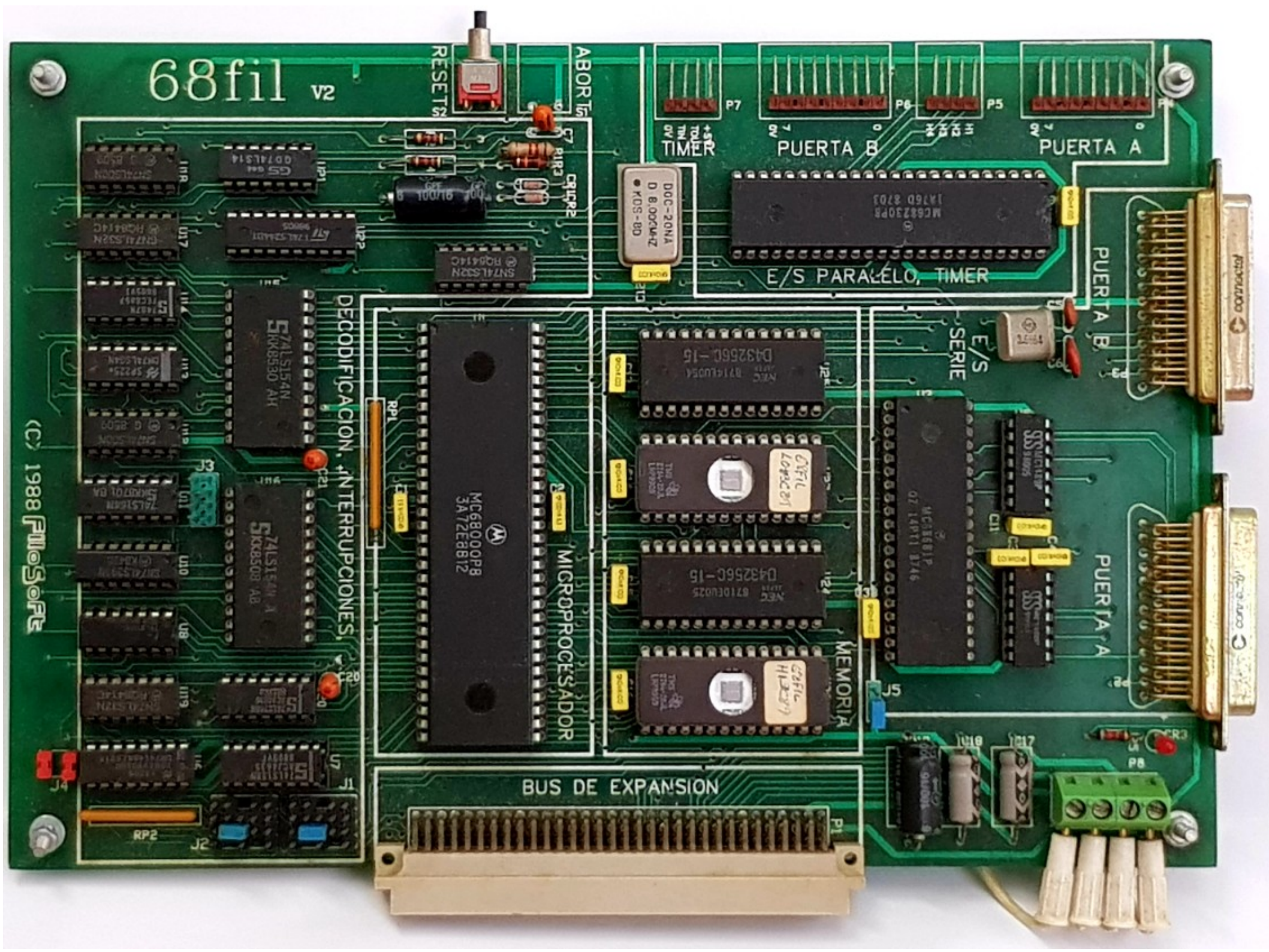


SITUACION DE LOS PUNTOS PARA CONEXION DE INTERRUPCIONES J1 Y J2



PRODUCTO	68fil
VERSION	v2
CIRCUITO	Sistema de interrupciones
FECHA	2-9-88
HOJA	6 DE 10

FilloSoft


68fil V2
RESET
ABORT
TIMER
PUERTA B
PUERTA A
E/S PARALELO, TIMER
DECODIFICACION, INTERRUPCIONES,
MICROPROCESADOR
MEMORIA
E/S SERIE
BUS DE EXPANSION
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