

## Cálculo de tiempos de ejecución (ciclos) (1) vs. (3) y (2) vs. (4)

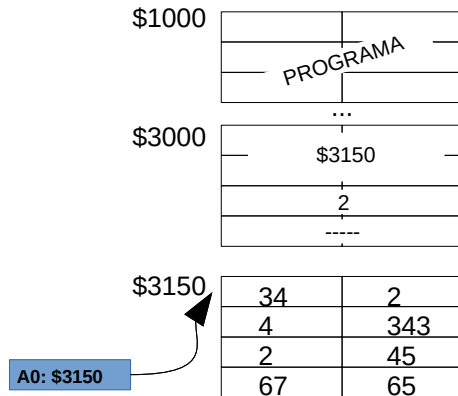
```

;asmsyntax=asm68k
CPU      68000

STRUCT   ORG      $3000
         DC.L     ARRAY
         DC.W     2
         DS.W     1

PROG     ORG      $1000
         MOVE.L   STRUCT,A0           ; (1)
         MOVE.W   STRUCT+4,D0        ; (1)
         MULU    #2,D0               ; (2)
         MOVE.W   (A0,D0.W),STRUCT+6 ; (1)
         TRAP    #15
         DC.W     0

ARRAY    ORG      $3150
         DC.W     34,2,4,343,23,45,67,65
    
```



```

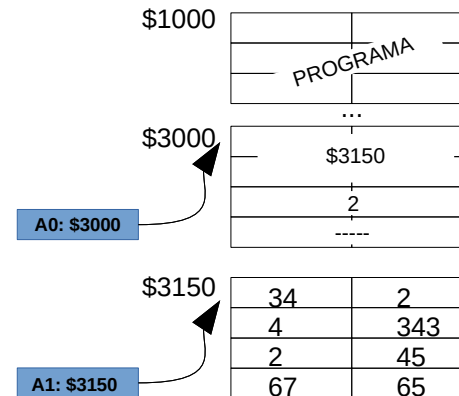
;asmsyntax=asm68k
CPU      68000

STRUCT   ORG      $3000
         DC.L     ARRAY
         DC.W     2
         DS.W     1

INDICE   EQU     4
RESULT   EQU     6

PROG     ORG      $1000
         LEA     STRUCT,A0           ; (3)
         MOVE.L   (A0),A1            ; (3)
         MOVE.W   INDICE4(A0),D0    ; (3)
         LSL.W    #1,D0              ; (4)
         MOVE.W   (A1,D0.W),RESULT(A0) ; (3)
         TRAP    #15
         DC.W     0

ARRAY    ORG      $3150
         DC.W     34,2,4,343,23,45,67,65
    
```



# BYTE

the small systems journal

APRIL 1981 Vol. 6, No. 4  
\$2.50 in USA/\$2.95 in Canada  
A McGraw-Hill Publication



**FUTURE COMPUTERS?**

Robert Tinney's cover for the April 1981 issue of *Byte* magazine Internet Archive



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have a higher screen resolution than Apple.

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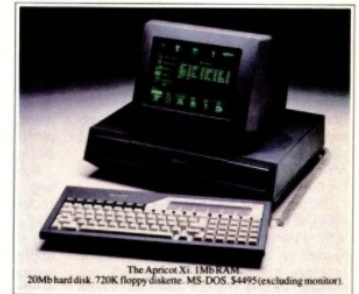
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Apricot, Inc., 3375 Scott Boulevard, Santa Clara, CA 95054. Call 800-227-6703, or in California 800-632-7979.

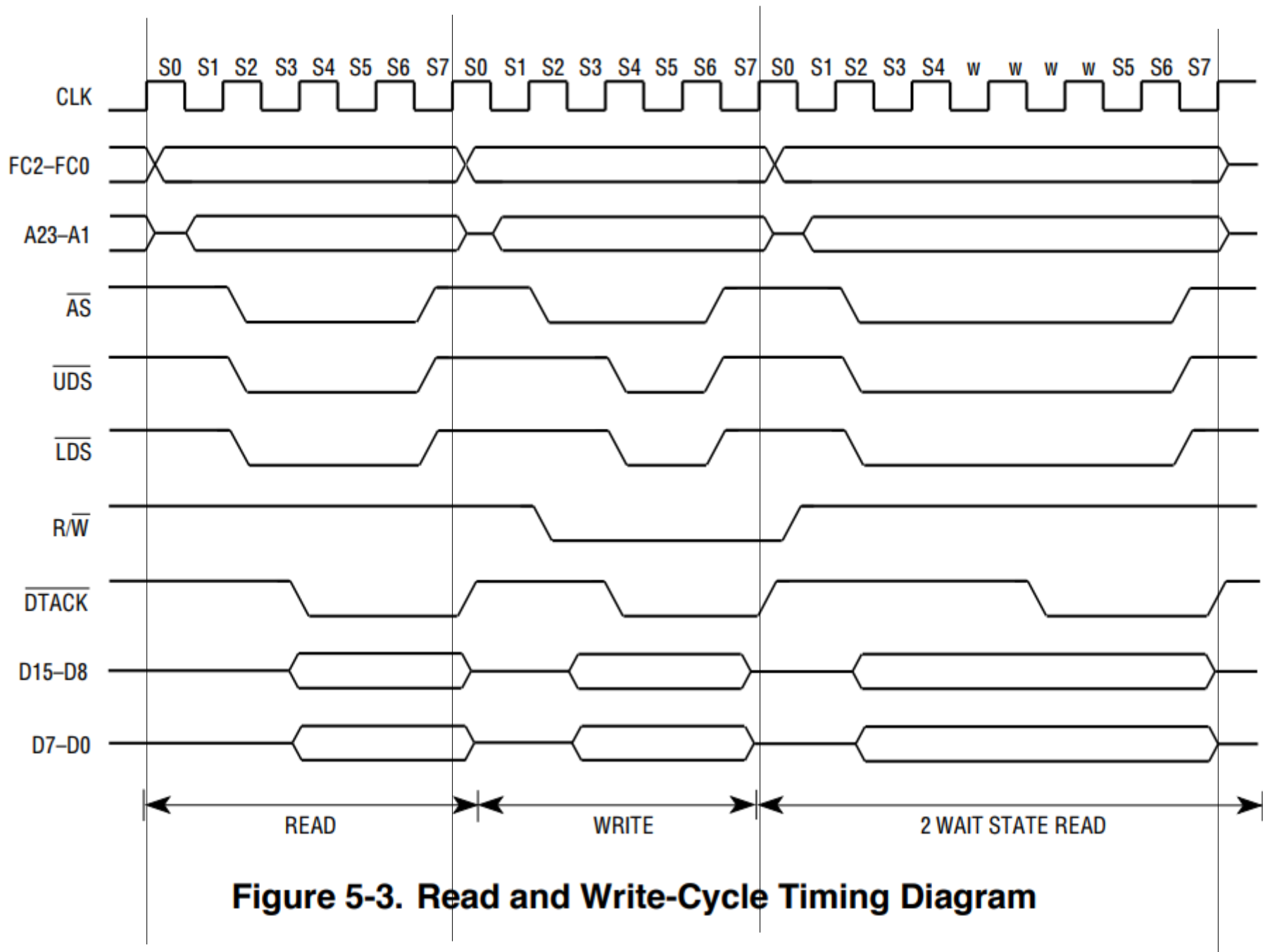


# change how American computer industry.

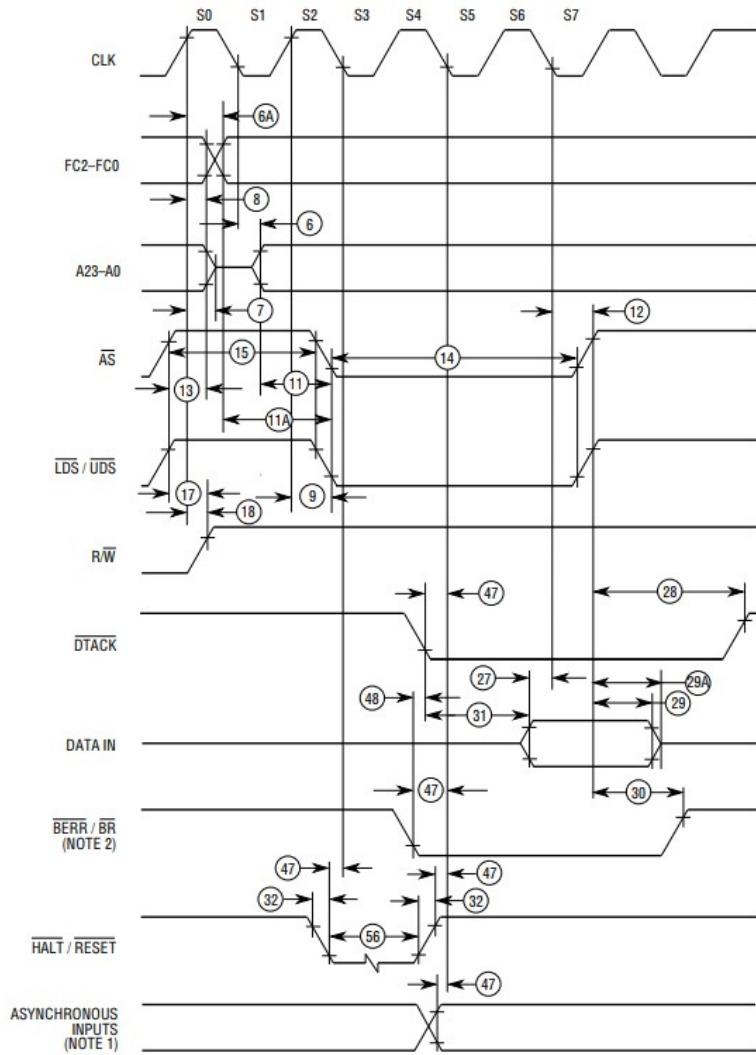


The Apricot Xi. 1MB RAM. 20Mb hard disk. 720K floppy diskette. MS-DOS. \$4495 (excluding monitor).

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We're changing how American business does business.



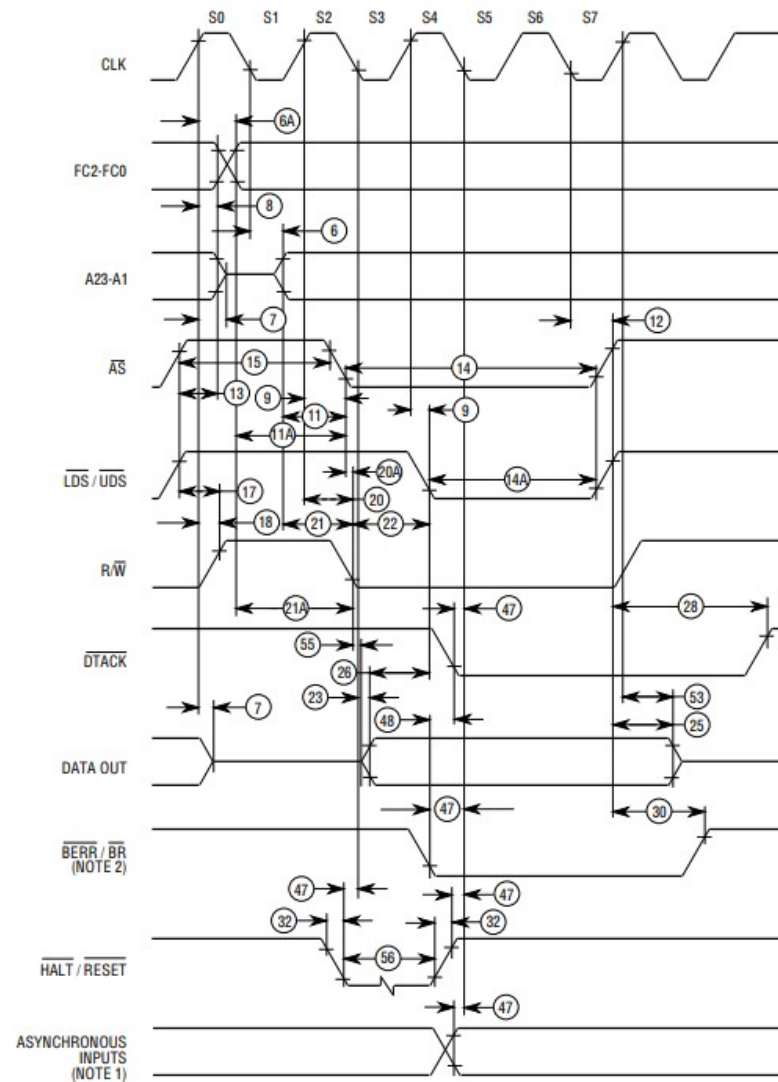
**Figure 5-3. Read and Write-Cycle Timing Diagram**



NOTES:

1. Setup time for the asynchronous inputs  $\overline{IPL2}$ – $\overline{IPL0}$  and  $\overline{AVEC}$  (#47) guarantees their recognition at the next falling edge of the clock.
2.  $\overline{BR}$  need fall at this time only to insure being recognized at the end of the bus cycle.
3. Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 V and 2.0 V.

**Figure 10-4. Read Cycle Timing Diagram**  
(Applies To All Processors Except The MC68EC000)



NOTES:

1. Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 V and 2.0 V.
2. Because of loading variations,  $\overline{R/W}$  may be valid after  $\overline{AS}$  even though both are initiated by the rising edge of  $S2$  (specification #20A).

**Figure 10-5. Write Cycle Timing Diagram**  
(Applies To All Processors Except The MC68EC000)