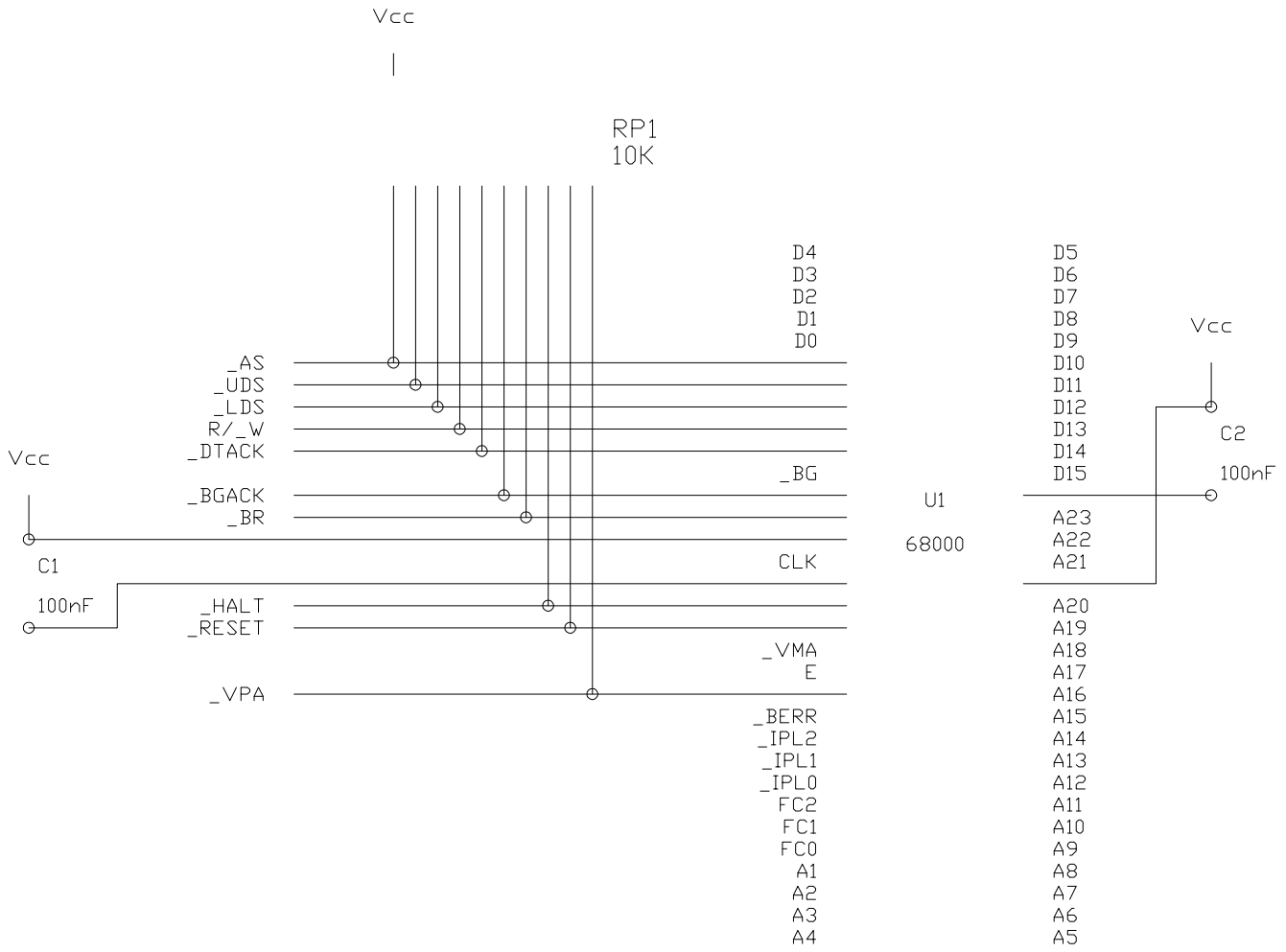
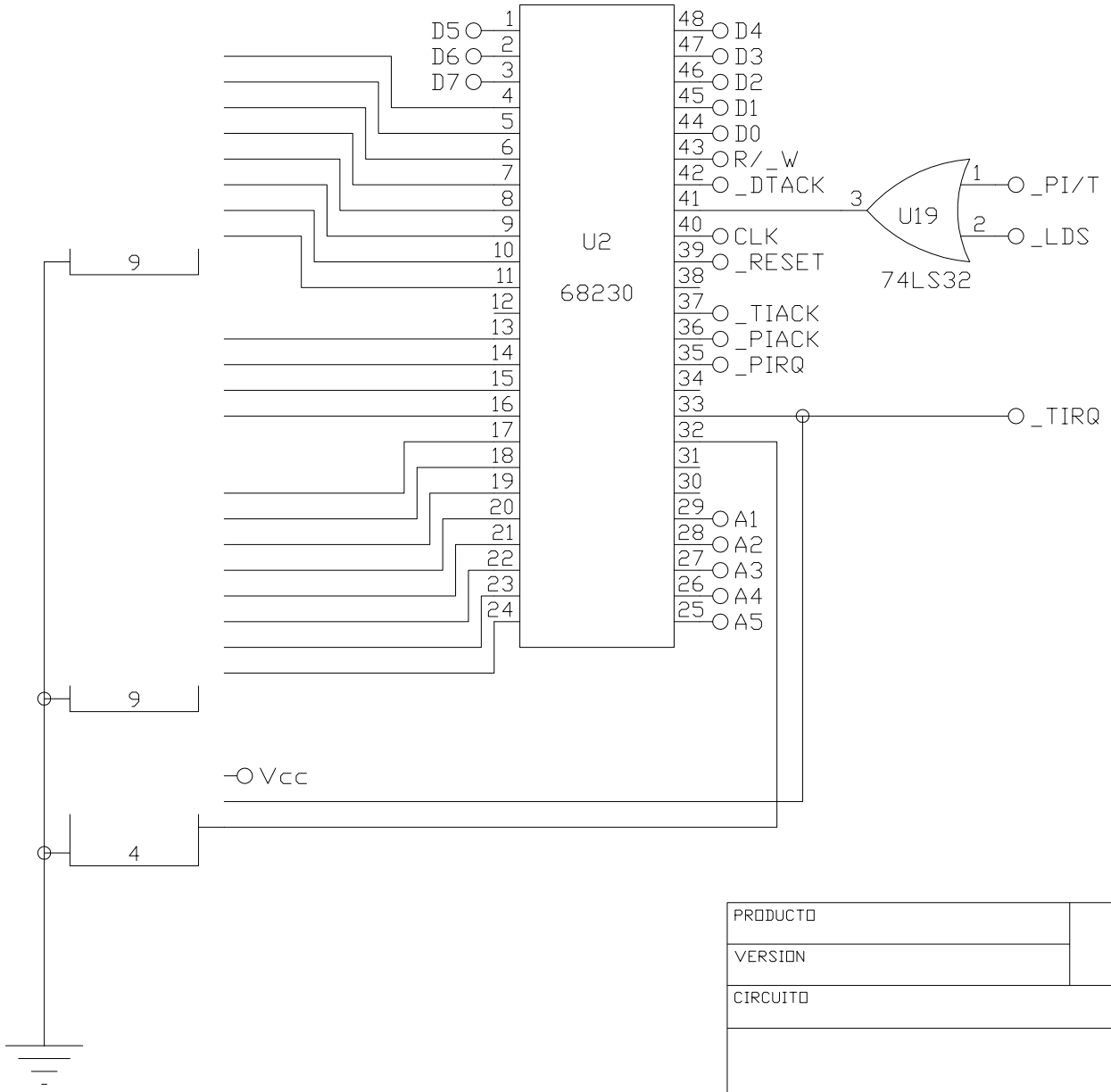
FiloSoft

*** 68fil - esquemas ***

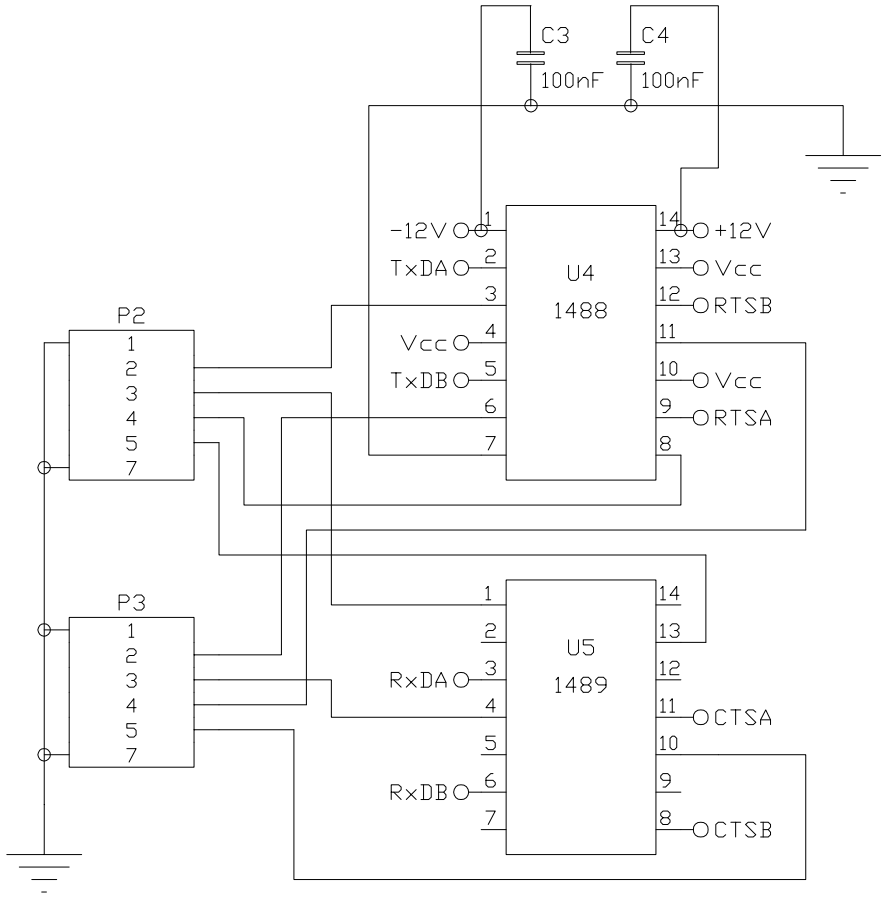
1- Microprocesador
2- Interface paralelo / timer
3- Comunicaciones asincronas
4- Memoria
5- Decodificacion de direcciones
6- Sistema de interrupciones
7- Generacion de CLK, DTACK, BERR
8- Generacion de RESET y HALT. Interrupcion ABORT
9- Conector de expansion
10- Alimentacion

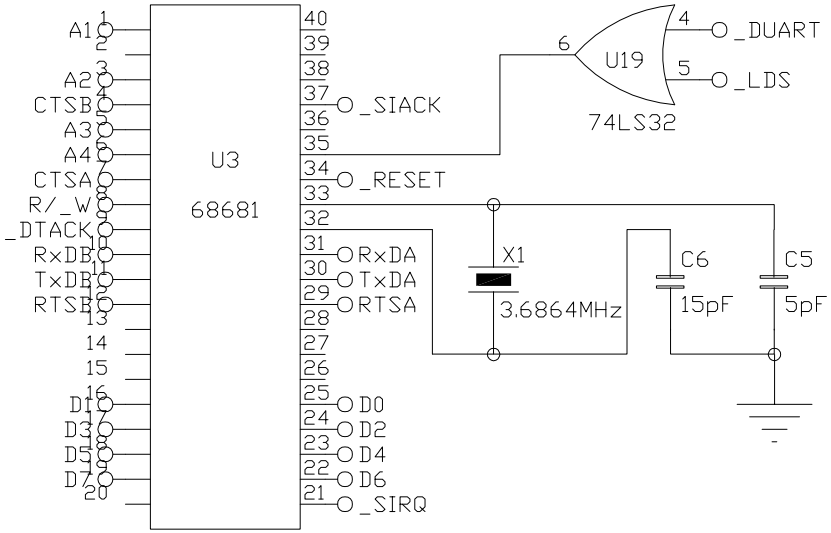


PRODUCTO	68fil
VERSION	v2
CIRCUITO	Microprocesador
FECHA	2-9-88
HOJA	1 DE 10



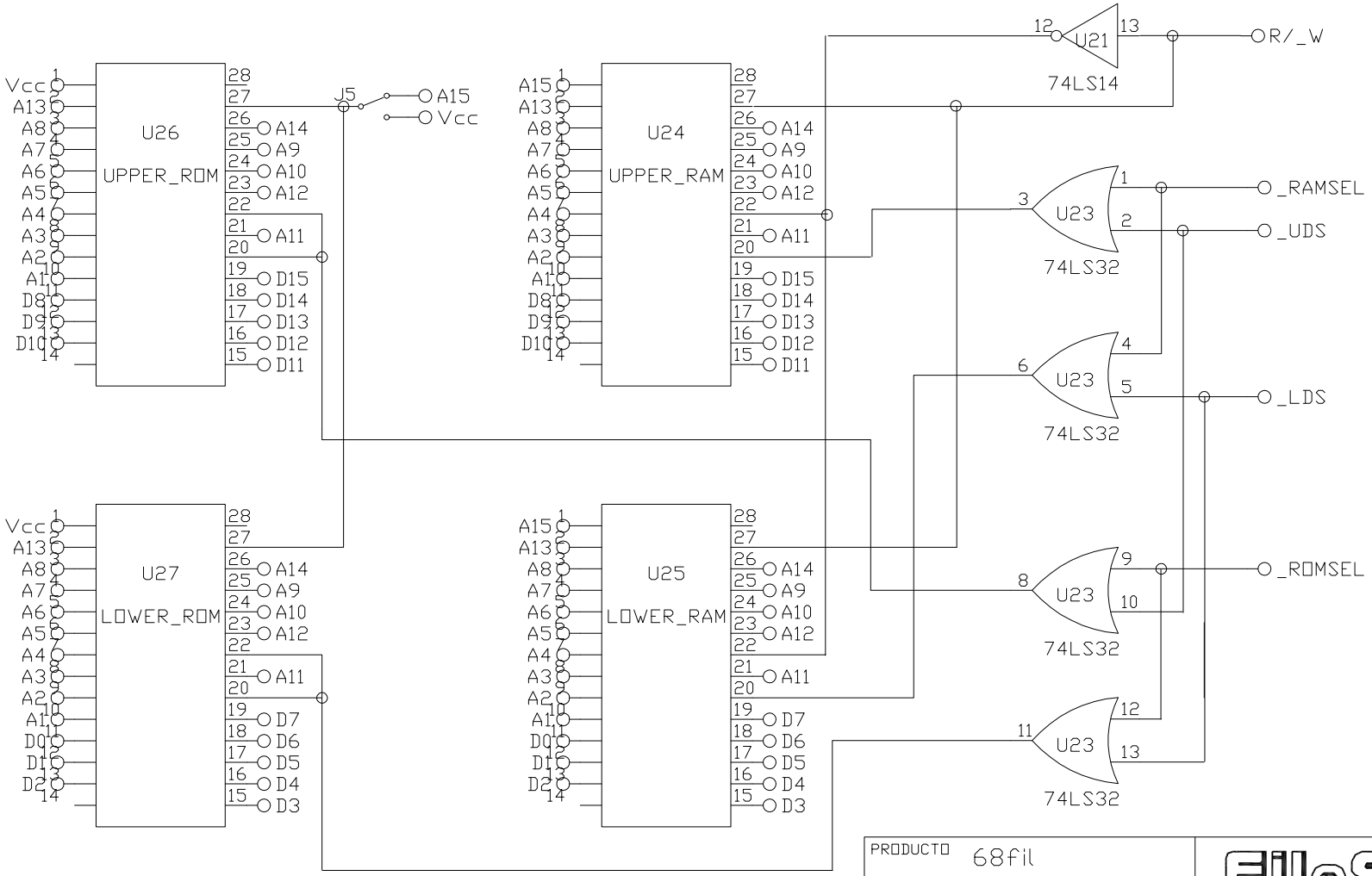
PRODUCTO	=
VERSION	
CIRCUITO	
	FECHA
	HOJA DE





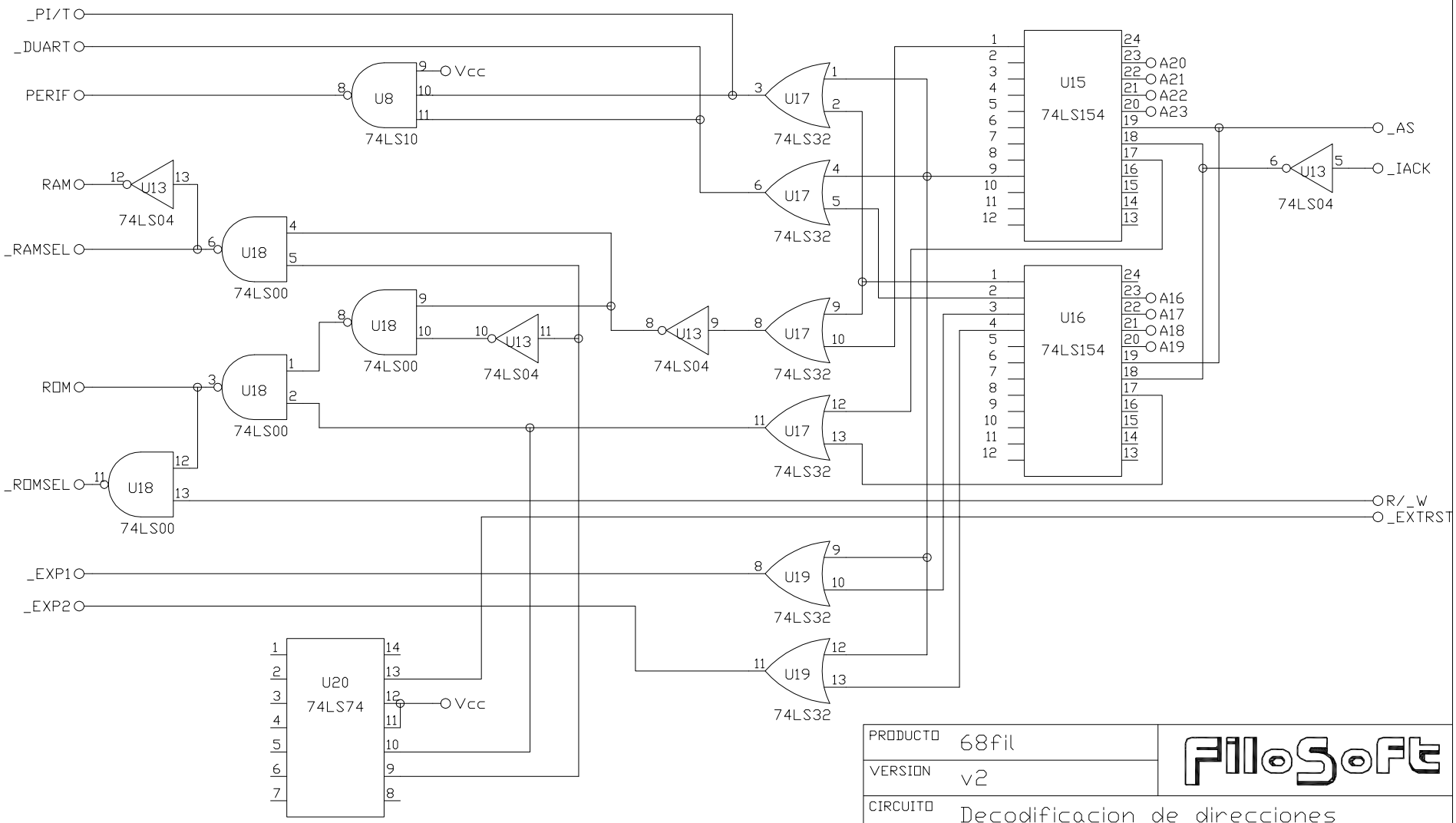
PRODUCTO	68fil
VERSION	v2
CIRCUITO	Comunicaciones asincronas
FECHA	2-9-88
HOJA	3 DE 10

FiloSoft



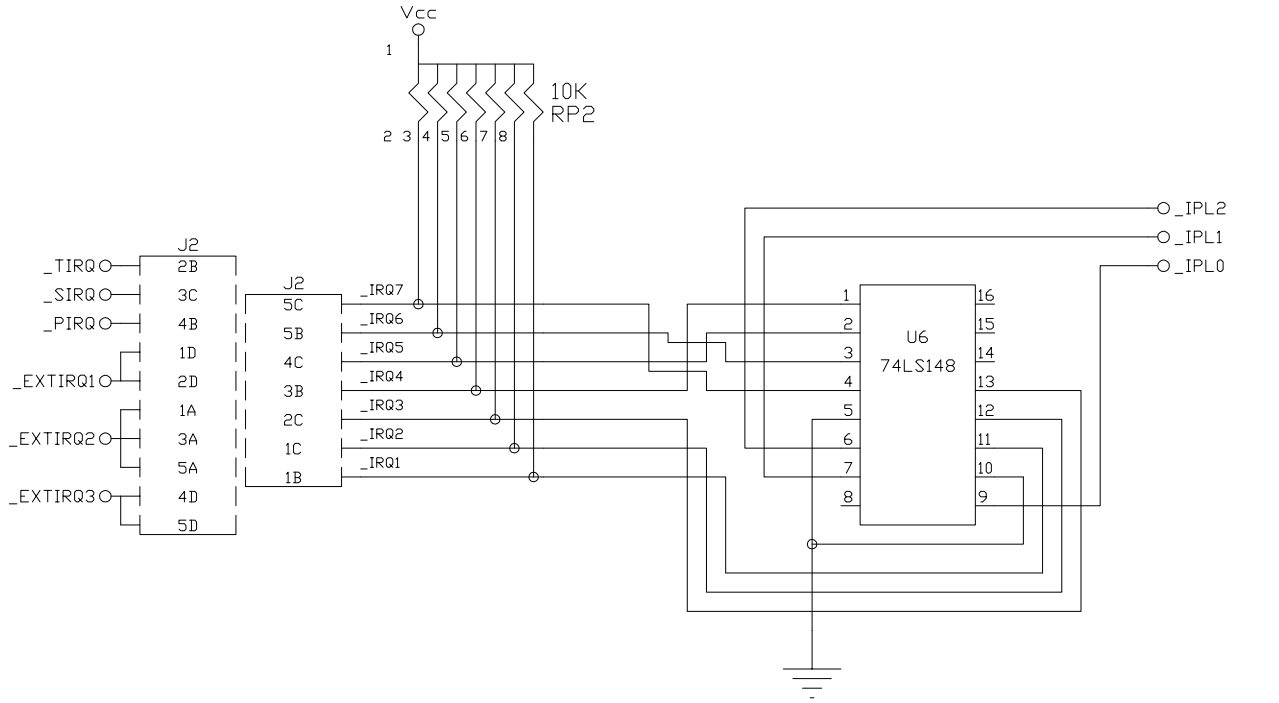
PRODUCTO	68fil
VERSION	v2
CIRCUITO	Memoria
FECHA	2-9-88
HOJA	4 DE 10

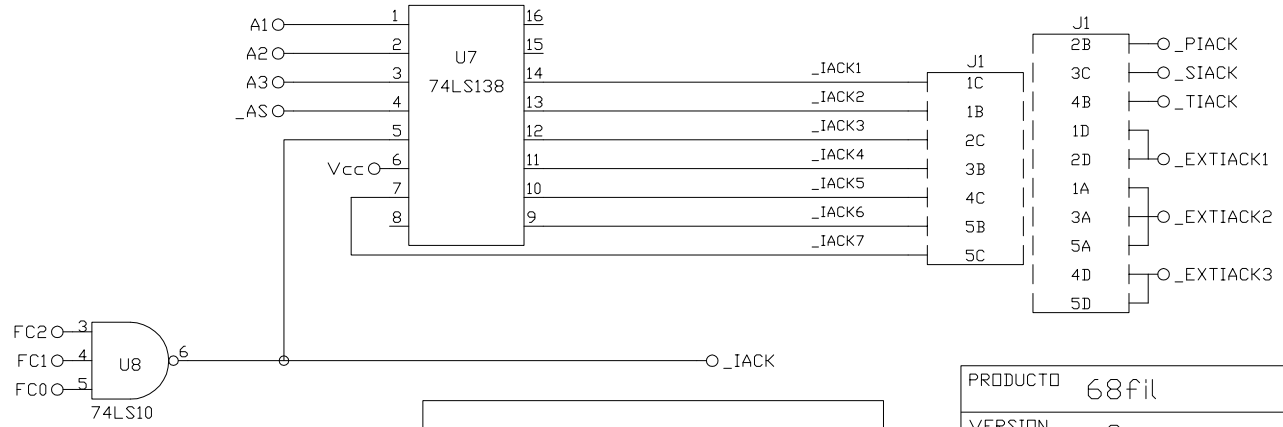
FiloSoft



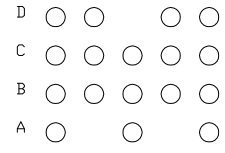
PRODUCTO	68fil
VERSION	v2
CIRCUITO	Decodificacion de direcciones
FECHA	2-9-88
HOJA	5 DE 10

FiloSoft



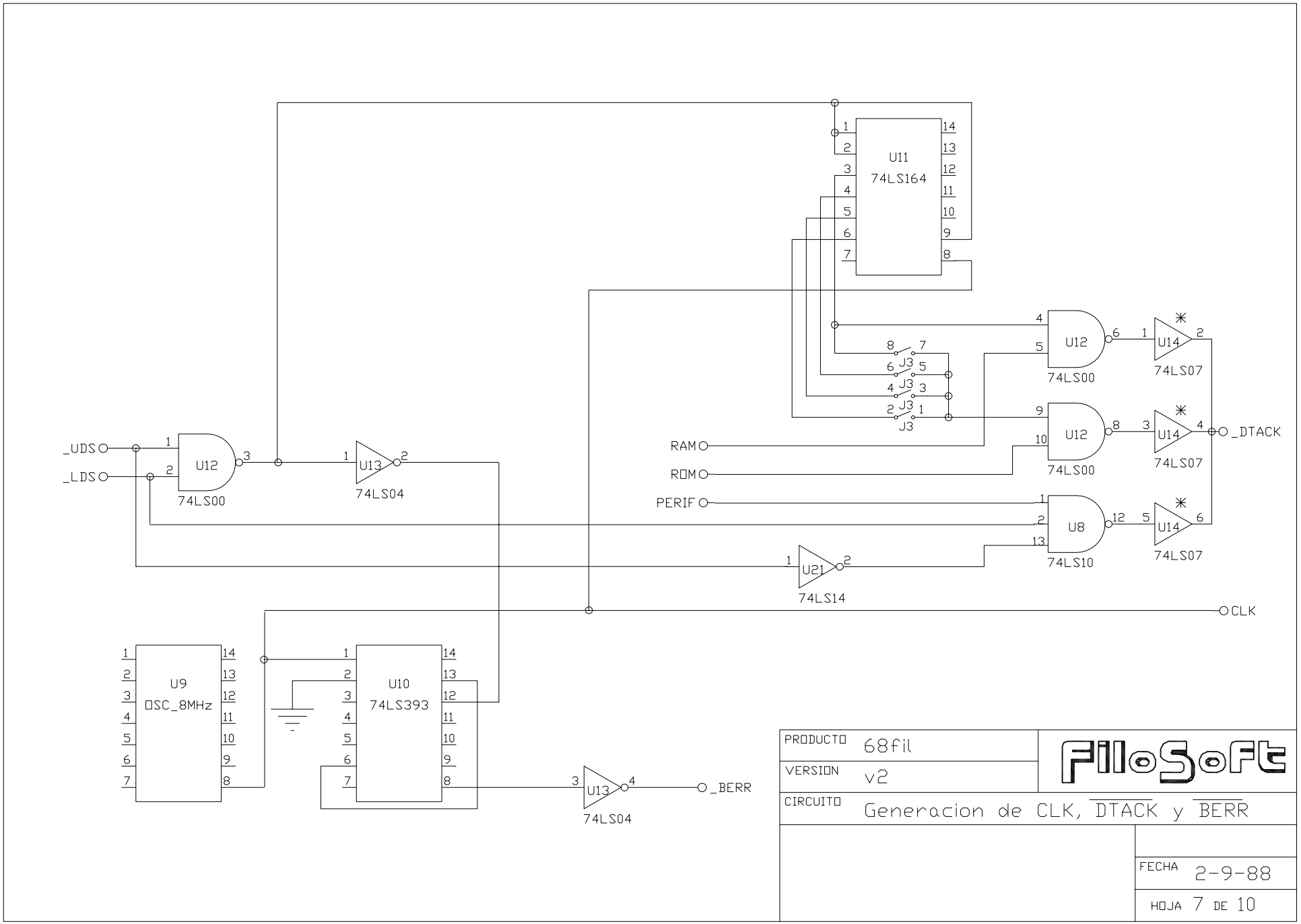


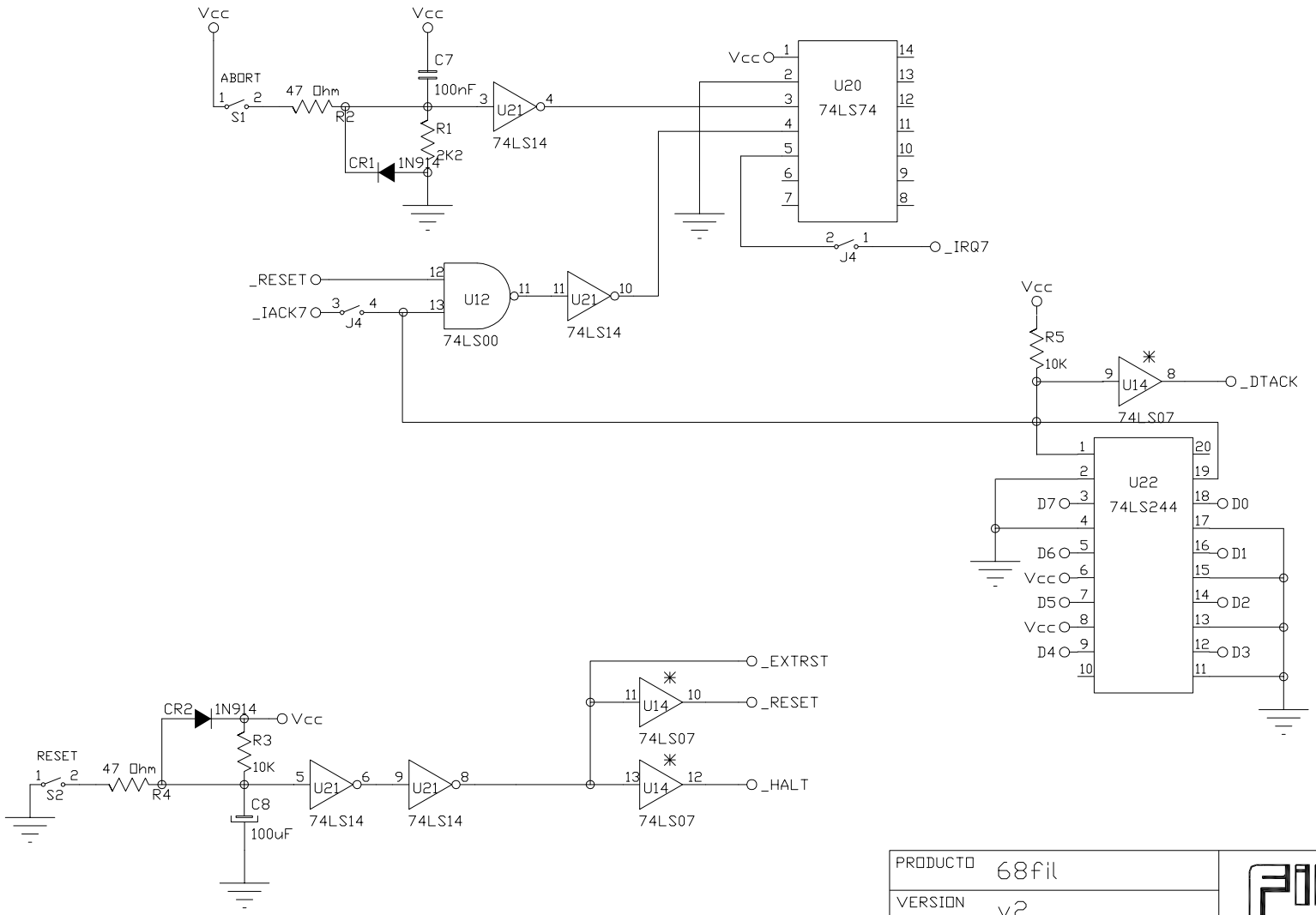
SITUACION DE LOS PUNTOS PARA CONEXION DE INTERRUPCIONES J1 Y J2



PRODUCTO	68fil
VERSION	v2
CIRCUITO	Sistema de interrupciones
FECHA	2-9-88
HOJA	6 DE 10

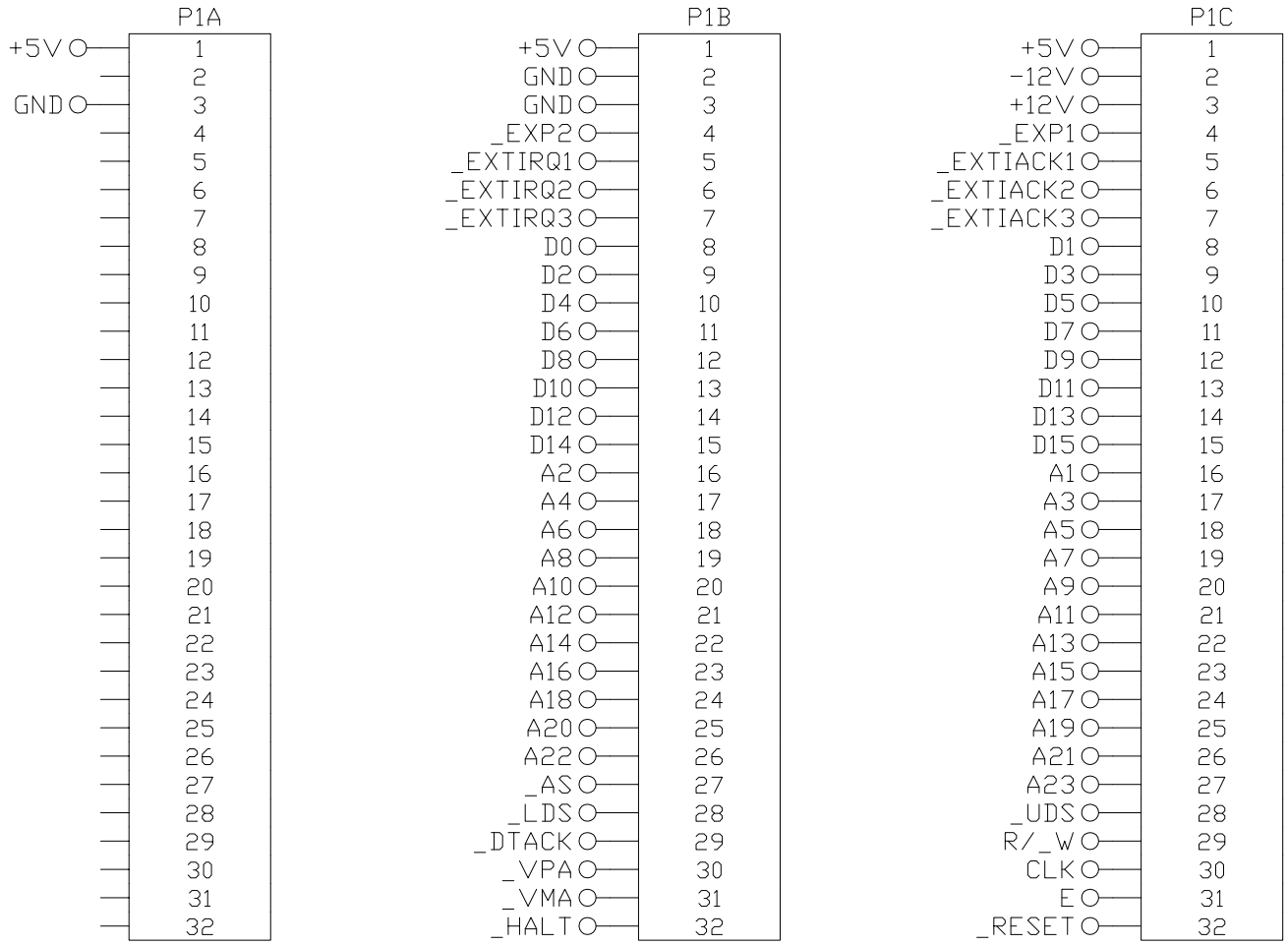
FiloSoft


U11
74LS164
U12
74LS00
U13
74LS04
U14
74LS07
U8
74LS10
U21
74LS14
U9
OSC_8MHz
U10
74LS393
J3
_UDS
_LDS
RAM
ROM
PERIF
_DTACK
CLK
_BERR
PRODUCTO 68fil
VERSION v2
CIRCUITO Generacion de CLK, DTACK y BERR
FECHA 2-9-88
HOJA 7 DE 10
FiloSoft



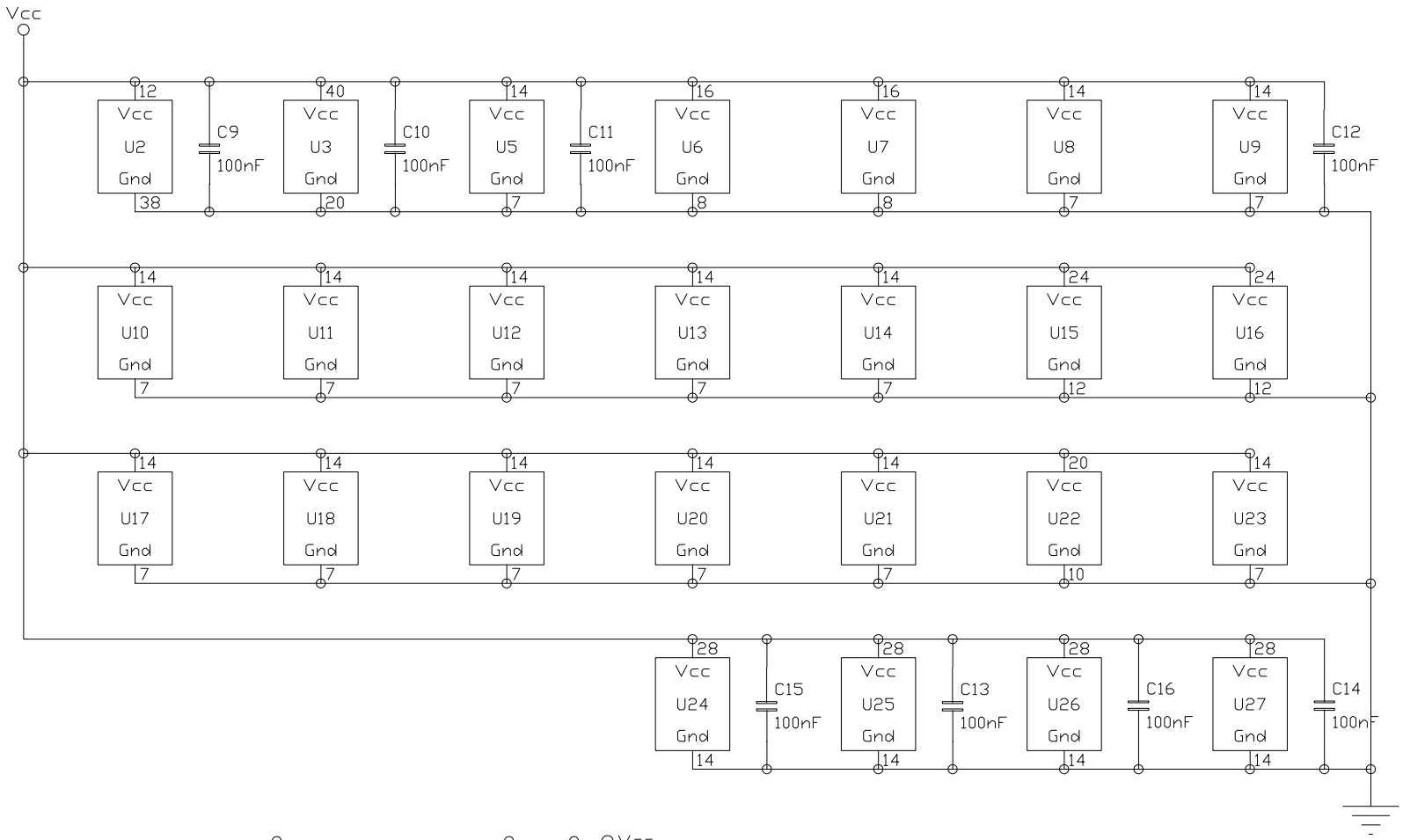
PRODUCTO	68fil
VERSION	v2
CIRCUITO	Generacion de $\overline{\text{RESET}}$ y $\overline{\text{HALT}}$. Interrupcion ABORT
FECHA	2-9-88
HOJA	8 DE 10

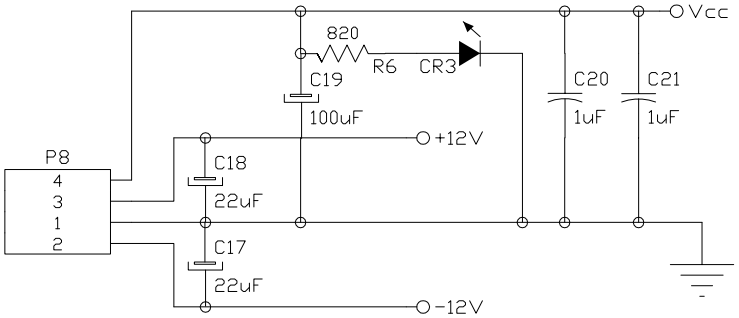
FiloSoft



PRODUCTO	68fil
VERSION	v2
CIRCUITO	Conector de expansion
FECHA	2-9-88
HOJA	9 DE 10

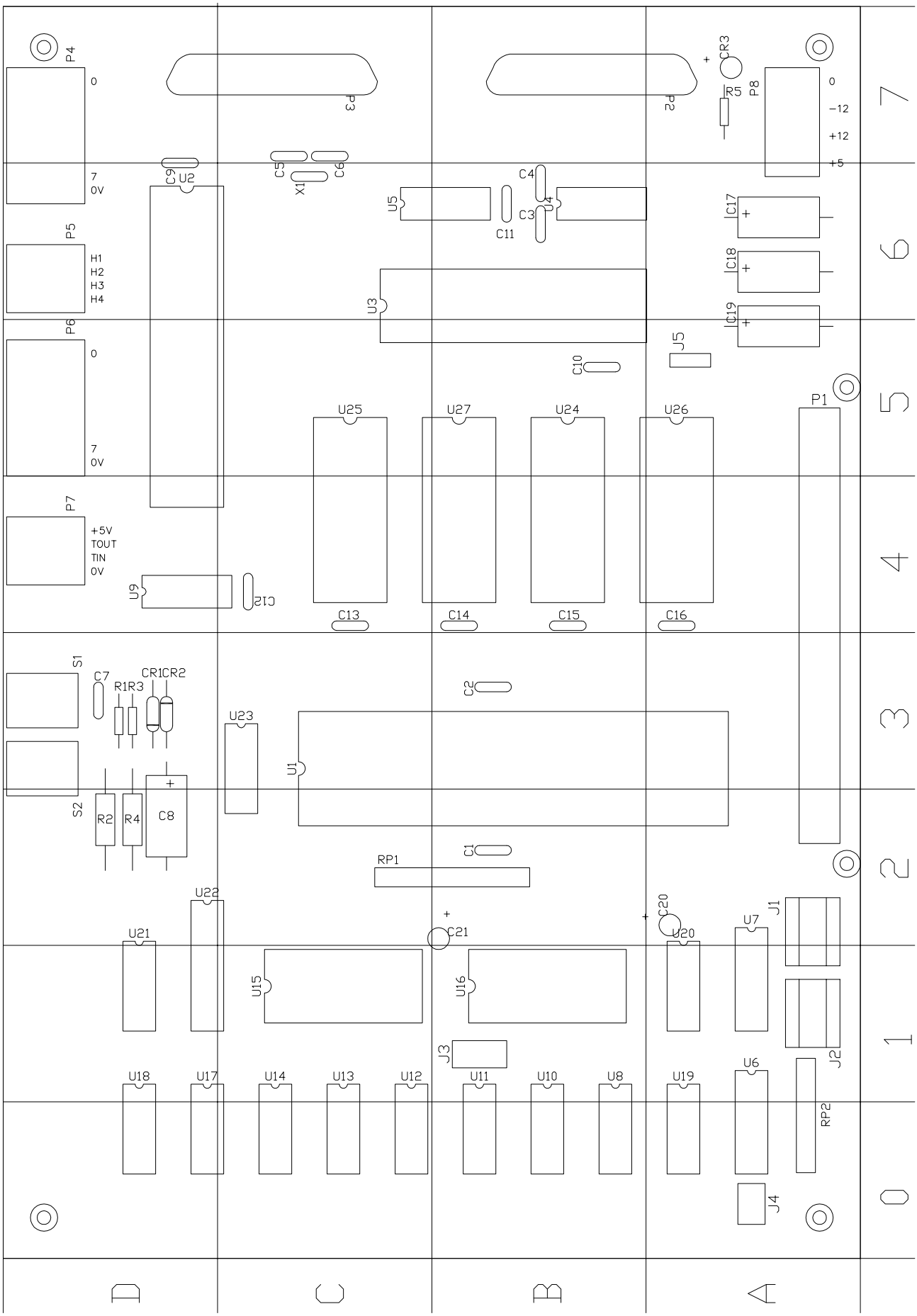
FiloSoft





PRODUCTO	68fil
VERSION	v2
CIRCUITO	Alimentacion
FECHA	2-9-88
HOJA	10 DE 10

FiloSoft


P4
0
7
0V
P5
H1
H2
H3
H4
P6
0
7
0V
P7
+5V
TOUT
TIN
0V
P3
P2
CR3
R5
P8
0
−12
+12
+5
C9
U2
C5
C6
X1
U5
C11
C4
C3
U4
U3
C10
U5
C17
C18
C19
U25
U27
U24
U26
P1
U9
C12
C13
C14
C15
C16
S1
C7
CR1
CR2
R1
R3
C2
U23
U1
S2
R2
R4
C8
RP1
C1
U22
U21
C21
C20
U20
U7
J1
U15
U16
J3
J2
U18
U17
U14
U13
U12
U11
U10
U8
U19
U6
RP2
J4
7
6
5
4
3
2
1
0
D
C
B
A